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# Comparison and Digital Circuit Analysis Based on Low Power Subthreshold Dual Mode Logic

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***Abstract***
In this brief, we propose new low power techniques such as Variable body bias method. This technique reduces the leakage power by increasing the body to source voltage of the sleep transistor in the design. By reducing the leakage power overall power of the design is reduced. The proposed logic switches between the active mode and sleep mode. To reduce the leakage current in sleep mode, the body to source voltage of the sleep transistor increased. To increase the voltage of Sleep transistor another transistor is connected to it. Average power and delay are the parameters compared between proposed logic to their CMOS and Dual Mode Logic counter parts in 180-nm process.

***Keywords***- Subthreshold , Dual Mode Logic, Variable Body Biasing

## I. INTRODUCTION

Reduction of power consumption became a primary focus in VLSI Design technology. Usage of huge mobile applications on a single device for long period also a reason to reduce power consumption of the devices. In VLSI designs power, speed and area are the most often used measures for determining the performance of the VLSI designs. Recently, digital subthreshold circuit design also became a promising method for ultra low power applications. Reduction in static power or dynamic power reduces the total power of the device. The different techniques are proposed to reduce the power consumption. But the various leakage power of the transistor plays a major role in power consumption. Reducing the leakage power benefits the total power consumption than reducing the static and dynamic powers without reducing their performance. The proposed logic can be operated in two modes: Sleep mode and active mode. The most common CMOS logic family uses to design the logic circuits along with a couple of transistors as header and footer. These transistors are connected as a new technique to vary the body effect of the transistor in two different modes.

"CMOS" refers to both a particular style of digital circuitry design and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. Since this advantage has increased and grown more important, CMOS processes and variants have come to dominate, thus the vast majority of modern integrated circuit manufacturing is on CMOS processes.

Another logic which comes under subthreshold leakage currents is the Dual Mode Logic .The basic DML gate architecture is composed of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal, as shown in Fig (1.1).

The basic Dual Mode Logic (DML) gate architecture is composed of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal. DML allow operation in two functional modes: static mode and dynamic mode. To operate the gate in dynamic mode, the Clock (Clk) is assigned, allowing two distinct phases: precharge and evaluation. During the precharge phase, the output is charged to high/low, depending on the topology of the DML gate. In the consequent evaluation phase, the output is evaluated according to the values at the gate inputs.

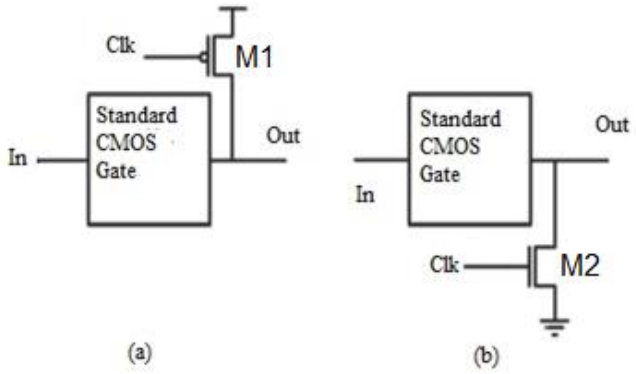


**Fig 1.1: DML (a) type-A topology (b) type-B topology**

The DML topologies are of two types, marked as, Type A and Type B. Type A has an added

p-MOS transistor that precharges the output to a logical "1" during the precharge phase. Type B has an added n-MOS that precharges the output to a logical "0". Dynamic logic gates are often implemented using a footer, which an additional transistor (optional). The Clk should be fixed high for Type A and constantly low for Type B topology. Chapter II explains the proposed method and chapter III shows the simulation results and chapter IV gives the conclusion.

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## II. PROPOSED METHOD

In the proposed method we introduce a new leakage power reduction technique named as "Variable Body Biasing". Normally, we have leakage power during idle (sleep) mode. By reducing the leakage power the total power dissipation of the technique is reduced. Thus to operate a logic design in sleep and active modes, a logic is used to control the design. In this proposed method we added the header (M1) and footer (M2) transistors between the pull-up network and pull-down network. By using these transistors the circuit forms as a conventional sleep transistor method.

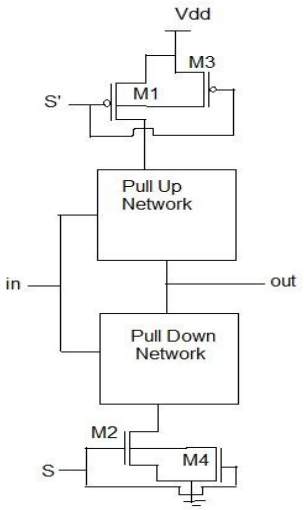


**Fig 2.1: Variable Body Bias method**

To reduce the leakage current in the sleep mode we ensured that threshold voltage of the sleep transistor is increased, we added a PMOS (M3) and an NMOS (M4) transistor as shown in the Fig2.1 during sleep mode PMOS (M2) is OFF so the body to source voltage of the pull up PMOS (M1) is higher than in the active mode.

The figure shown in the Fig 2.2 is a sleep transistor without variable body bias technique. Here the transistor source terminal is connected to the Vdd and drain terminal is connected to the virtual Vdd above the pull up network. When the sleep signal(S') is low the transistor is turned ON so the circuit will work normally. But when sleep signal(S') is high the transistor is turned OFF but a small leakage current flows through the transistor which is subthreshold leakage causes power dissipation.

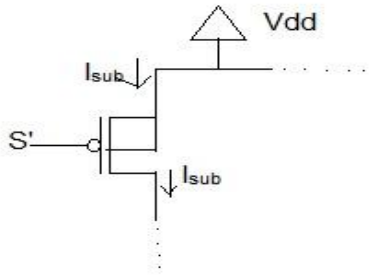


**Fig 2.2: sleep transistor without variable body biasing transistor.**

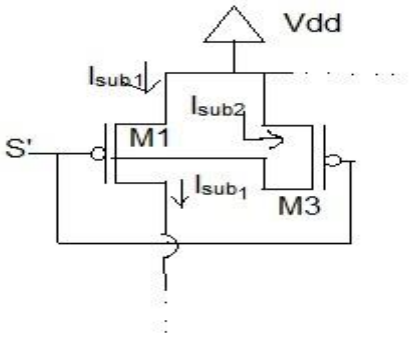


**Fig 2.3: sleep transistor with variable body biasing**

The figure 2.3 shows the variable body biasing technique which avoids the subthreshold leakage current during idle mode. As the drain terminal of M3 transistor is connected to body (fourth terminal of the transistor) of the transistor M1, when the sleep signal(S') is low the circuit works normally but when the sleep signal(S') is high the M3 transistor is OFF which causes to increase the threshold voltage of the transistor M1. Hence the M1 transistor is turned off fully no current flows through the circuit.

For a turned off single transistor leakage current (Isub0) can be expressed as follows

$$Isub0 = Ae^{\frac{1}{nV_\theta}(V_{gs0}-V_{th0}-\gamma V_{sb0}+\eta V_{ds0})}(1 - e^{-V_{ds0}/V_\theta})$$

Where

$$A = \mu_0 C_{0x}\left(\frac{W}{L_{eff}}\right)V_\theta^2 e^{1.8}$$

$n$ is the subthreshold swing coefficient and $V_\theta$ is the thermal voltage. $V_{gs}$, $V_{th0}$, $V_{sb}$ and $V_{ds}$ are the gate-to-source voltage, the zero-bias threshold voltage, the source-to-base voltage and the drain-to-source voltage, respectively. $\gamma$ is the body-bias effect coefficient, and $\eta$ is the Drain Induced Barrier Lowering (DIBL) coefficient. $\mu_0$ is zero-bias

mobility, $C_{ox}$ is the gate-oxide capacitance, W is the width of the transistor, and $L_{eff}$ is the effective channel length. From the equation we see that leakage current (Isub0) decreases as $V_{sb0}$ increases. As a result of Body effect, $V_{th}$ also increases which lowers the performance. During the active mode, the performance is improved when the transistor (M3) is ON which makes the $V_{th}$ of the pull up transistor (M1) lower again. The same operation is applicable for the pull down transistors (M2 and M4).

## III. SIMULATION RESULTS

The proposed logic is designed using three consecutive NAND and NOR gates and compared propagation delay and average power with the CMOS and DML logic families. The design is carried out in 180nm Tanner EDA tools. The proposed method works in active mode (sleep signal is 1) and shows undetermined value during sleep mode (sleep signal is 0).

### 1) Design of three consecutive NAND gates using proposed method:

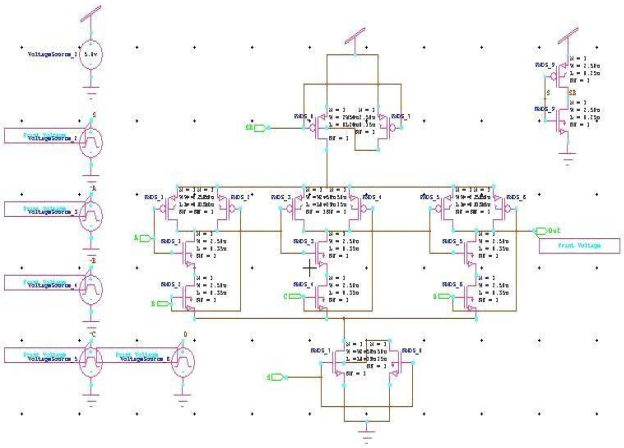

**Fig 3.1: Three consecutive NAND gates using Proposed method**

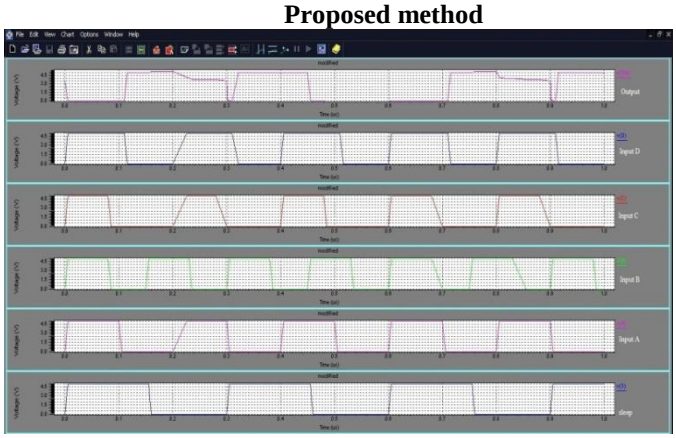

**Fig 3.2: Output waveforms of three consecutive NAND gates using proposed method**

### 2) Design of three consecutive NOR gates using proposed method:

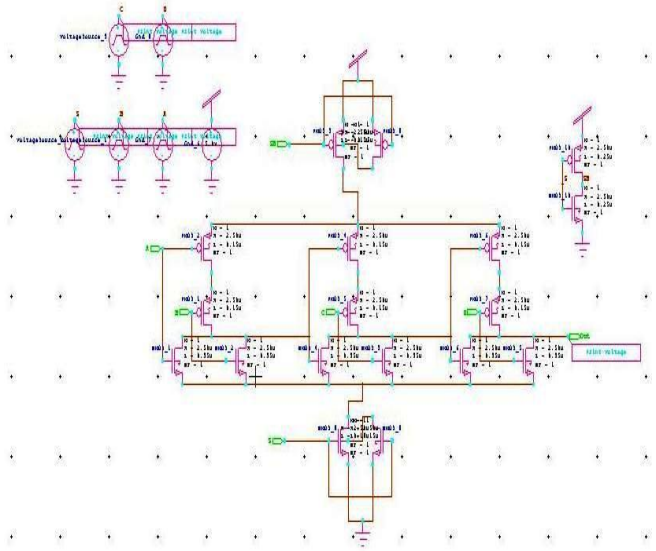

**Fig 3.3: Three consecutive NOR gates using Proposed method**

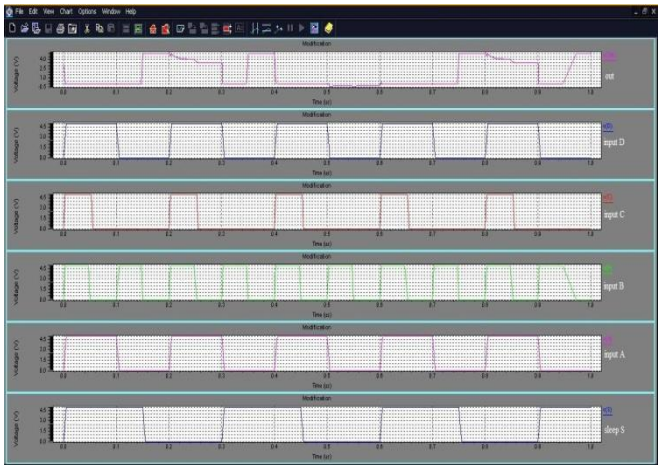

**Fig 3.4: Output waveforms of three consecutive NOR gates using proposed method**

**Table 1: Comparison of Average Power and Delay**

| Logic | Circuit | Average Power(mw) | Delay(sec) |
|---|---|---|---|
| CMOS | NAND | 0.67 | 2.25 |
| DML Type A | NAND | 0.28 | 2.12 |
| DML Type B | NAND | 0.25 | 2.14 |
| Proposed | NAND | 0.07 | 1.76 |
| **Logic** | **Circuit** | **Average Power(mw)** | **Delay(sec)** |
| CMOS | NOR | 0.67 | 1.89 |
| DML Type A | NOR | 0.23 | 1.59 |
| DML Type B | NOR | 0.36 | 1.58 |
| Proposed | NOR | 0.10 | 1.34 |

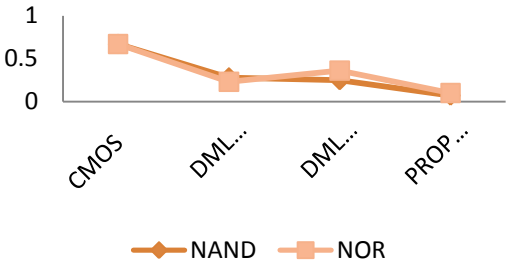


**Fig 3.5: Comparison of power (mw)**

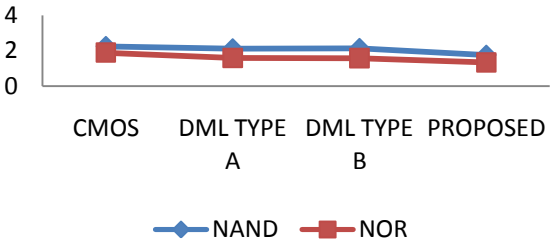


**Fig 3.6: Comparison of delay**

## IV. CONCLUSION

The proposed design technique for minimizing the leakage power must be developed along with the device scaling. To reduce the standby leakage power, this paper has presented design technique that generates the optimal Body scaling during standby mode. Miniaturization of CMOS technology achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power. Our Variable Body Biasing approach shows improved results in terms of static power and dynamic power. It gives the CMOS circuit designers another option in designing integrated circuits more efficiently. These designs carried out in 180nm technology Tanner EDA tools.

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